

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 04-164372

(43)Date of publication of application : 10.06.1992

(51)Int.Cl.

H01L 29/788
H01L 27/115
H01L 29/792

(21)Application number : 02-292573

(71)Applicant : TOSHIBA CORP
TOSHIBA MICRO ELECTRON KK

(22)Date of filing : 29.10.1990

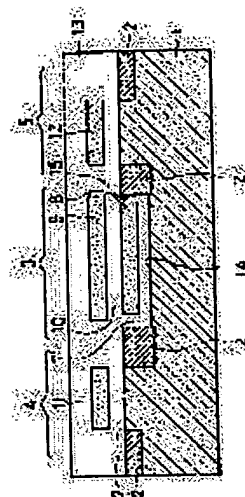
(72)Inventor : TANEDA HIROTO

(54) SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:

PURPOSE: To improve flatness of the upper surface of a substrate, and prevent disconnection of a metal wiring formed on an interlayer insulating film, by burying the bottom part of a floating gate electrode in a trench formed on the surface of an integrated circuit board.

CONSTITUTION: A trench 14 is formed between two source-drain regions of an information storage transistor 3 on the element region surface of an integrated circuit board. A gate insulating film 7' is formed also on the inner wall of the trench 14, and at least the bottom part of the floating gate electrode 8 is buried in the inside of the trench 14, via the gate insulating film 7'. A thin tunnel film 15 is formed between a part of the side surface of the floating gate electrode 8 and a part of the inner side surface of the trench 14. Since, in this manner, at least the bottom part of the floating gate electrode 8 is buried in the trench 14 formed on a part of the integrated circuit board surface, the level difference on the substrate upper surface is reduced, and the flatness of the substrate upper surface is improved.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office